ADTEC

PC5-4800 8GB non-ECC 1Rank SO-DIMM

Note: ADTEC Corporation reserves the right to change products and specifications without notice.

Description

This Memory Module is PC5-4800 8GB (x64, 1Rank) 262-pin Small Outline Dual In-Line Memory Module (SO-DIMM).

Feature

- 262-pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- Module Height: 30mm
- DDR5 functionality and operations supported as defined in the component data sheet
- Fast data transfer rates: PC5-4800
- VIN_BULK from Host = 5.0V (NOM)
- DRAM V_{DD}/V_{DDQ} from PMIC = 1.1V (NOM)
- DRAM V_{PP} from PMIC = 1.8V (NOM)
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- Temperature range
  - — Operation 0℃ ≦ Tc ≦ 85℃※
    Storage -55℃ ≦ Tc ≦ 100℃

    ※Some applications require operation of the Extended Temperature Range between 85℃ and 95℃ case temperature.
    Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 1.95us.

- PCB
  - — JEDEC compliant
  - — Flammability meets UL94V-0
    Material FR4
    Plating Ni= 2.00μm MIN
    Au= 0.76μm MIN
  - — Solder resist Halogen free
  - — Gold edge contacts and chamfer the corners

- RoHS2 compliant

DRAM

- Part Number: H5CG46AGBDX017
- Vendor: SK Hynix
- The DDR5 SDRAM is defined in JESD79-5.

PMIC

- Part Number: RTQ5132
- Vendor: RICHTEK
- The PMIC is defined in JESD301-2.

Pin Description

Pin Name	Description
CA0_A - CA12_A, CA0_B - CA12_B	SDRAM Command/Address bus
CS0_A_n, CS0_B_n	SDRAM Chip Select
DQ0_A - DQ31_A, DQ0_B - DQ31_B	DIMM memory data bus
DQS0_A_t – DQS3_A_t, DQS0_B_t – DQS3_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS3_A_c, DQS0_B_c – DQS3_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n - DM3_A_n, DM0_B_n- DM3_B_n	SDRAM data masks
CK0_A_t, CK0_B_t	SDRAM clocks (positive line of differ- ential pair)
CK0_A_c, CK0_B_c	SDRAM clocks (negative line of differ- ential pair)
HSCL	Host SidebandBus clock
HSDA	Host SidebandBus data
HSA	Host SidebandBus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a known State
VIN_BULK	5V power input supply to the PMIC for analog circuits
VSS	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	Power Enable
RFU	Reserved for future use

Note:
DDR5 SODIMM has 2 channels (channel-A and channel-B) of signal bus.The signals with suffix:_A (e.g. DQ0_A) are for channel-A, and the signals with suffix:_B (e.g.DQ0_B) are for channel-B

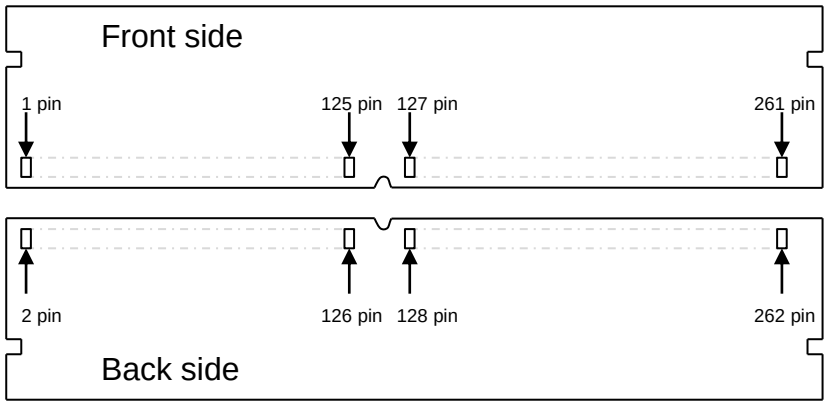
Input / Output Functional Description

Symbol	Type	I/O Level	Description
CK0_A_t, CK0_A_c, CK0_B_t, CK0_B_c	Input	VDD	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B - CA12_B	Input	VDD	**Command/Address Inputs:** CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins mat not be interchanged between devices on the same bus.
CS0_A_n, CS0_B_n	Input	VDD	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input/ Output	VDDQ	**Data Input/Output:** Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS0_A_t – DQS3_A_t DQS0_A_c – DQS3_A_c DQS0_B_t – DQS3_B_t DQS0_B_c – DQS3_B_c	Input/ Output	VDDQ	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n-DM3_A_n, DM0_B_n-DM3_B_n	Input	VDDQ	**Input Data Mask:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. .
ALERT_n	Input/ Output	VDD	**Alert:** If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	VDD	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	1.0V	**Host SidebandBus bus clock**, supplied by the controller.
HSDA	Input/ Output	1.0V	**Host SidebandBus data**, connected from the controller to Hub or Host bus Target devices.
HSA	Input	2.1V max	**Host SidebandBus bus device ID address pin**; input to a hub or other client device to distinguish between identical devices in the I3C-Basic/I2C address range.
RFU			Reserved for Future Use. No on DIMM electrical connection is present.

Input / Output Functional Description

Symbol	Type	I/O Level	Description
PWR_GOOD	Input/ Output	Open Drain	**Power good indicator.** Open Drain output. The PMIC floats this pin high when VIN_BULK input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_BULK input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
PWR_EN	Input	3.3V	**PMIC Enable.** When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. this signal is connected to PMIC‘s VR_EN pin.
VIN_BULK	Supply	5V	**5V power input supply** to the PMIC for analog circuits.
VSS	Supply		**Ground**

Pin Connection



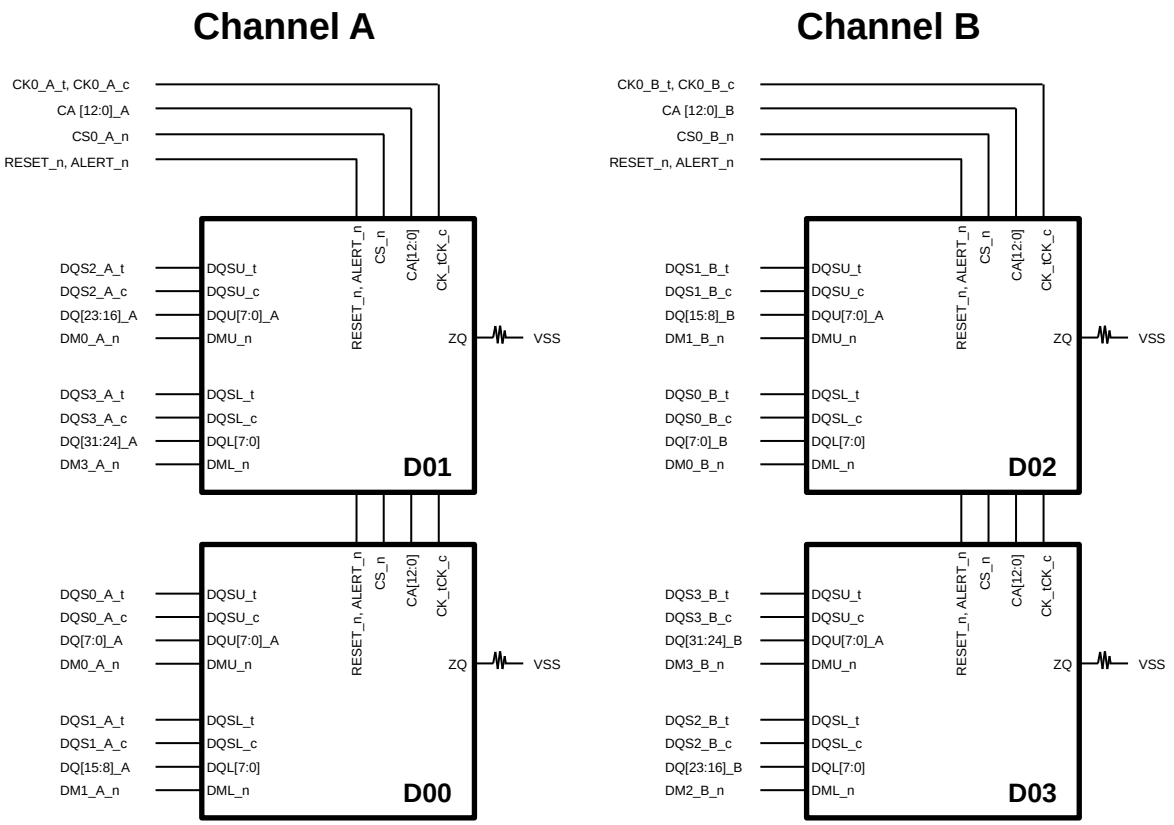
Pin Assignment

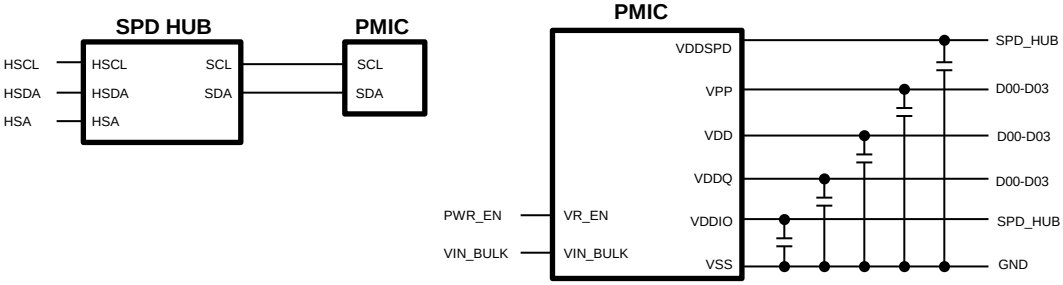
DDR5 SO-DIMM Front							
Pin#	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**
1	VIN_BULK	67	VSS	131	CK0_A_t	197	VSS
3	VIN_BULK	69	DQ22_A	133	CK0_A_c	199	DQ8_B
5	RFU	71	VSS	135	VSS	201	VSS
7	PWR_GOOD	73	DQ24_A	137	CK0_B_t	203	DQ10_B
9	VSS	75	VSS	139	CK0_B_c	205	VSS
11	DQ0_A	77	DQ26_A	141	VSS	207	DQS1_B_c
13	VSS	79	VSS	143	RFU	209	DQS1_B_t
15	DQ2_A	81	DQS3_A_c	145	CA11_B	211	VSS
17	VSS	83	DQS3_A_t	147	VSS	213	DQ12_B
19	DM0_A_n	85	VSS	149	CA9_B	215	VSS
21	VSS	87	DQ28_A	151	CA7_B	217	DQ14_B
23	DQ4_A	89	VSS	153	VSS	219	VSS
25	VSS	91	DQ30_A	155	CA5_B	221	DQ16_B
27	DQ6_A	93	VSS	157	CA3_B	223	VSS
29	VSS	95	NC	159	VSS	225	DQ18_B
31	DQ8_A	97	VSS	161	CS0_B_n	227	VSS
33	VSS	99	NC	163	RESET_n	229	DM2_B_n
35	DQ10_A	101	VSS	165	NC	231	VSS
37	VSS	103	NC	167	VSS	233	DQ20_B
39	DQS1_A_c	105	VSS	169	NC	235	VSS
41	DQS1_A_t	107	CA0_A	171	NC	237	DQ22_B
43	VSS	109	CA1_A	173	VSS	239	VSS
45	DQ12_A	111	VSS	175	NC	241	DQ24_B
47	VSS	113	CA2_A	177	VSS	243	VSS
49	DQ14_A	115	CA4_A	179	DQ0_B	245	DQ26_B
51	VSS	117	VSS	181	VSS	247	VSS
53	DQ16_A	119	CA6_A	183	DQ2_B	249	DQS3_B_c
55	VSS	121	CA8_A	185	VSS	251	DQS3_B_t
57	DQ18_A	123	VSS	187	DM0_B_n	253	VSS
59	VSS	125	CA10_A	189	VSS	255	DQ28_B
61	DM2_A_n	**Key**		191	DQ4_B	257	VSS
63	VSS	127	CA12_A	193	VSS	259	DQ30_B
65	DQ20_A	129	VSS	195	DQ6_B	261	VSS

Pin Assignment

DDR5 SO-DIMM Back							
Pin#	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**	**Pin#**	**Pin Name**
2	HSA	68	DQ21_A	132	NC	198	DQ7_B
4	HSCL	70	VSS	134	NC	200	VSS
6	HSDA	72	DQ23_A	136	VSS	202	DQ9_B
8	PWR_EN	74	VSS	138	NC	204	VSS
10	VSS	76	DQ25_A	140	NC	206	DQ11_B
12	DQ1_A	78	VSS	142	VSS	208	VSS
14	VSS	80	DQ27_A	144	CA12_B	210	DM1_B_n
16	DQ3_A	82	VSS	146	CA10_B	212	VSS
18	VSS	84	DM3_A_n	148	VSS	214	DQ13_B
20	DQS0_A_c	86	VSS	150	CA8_B	216	VSS
22	DQS0_A_t	88	DQ29_A	152	CA6_B	218	DQ15_B
24	VSS	90	VSS	154	VSS	220	VSS
26	DQ5_A	92	DQ31_A	156	CA4_B	222	DQ17_B
28	VSS	94	VSS	158	CA2_B	224	VSS
30	DQ7_A	96	NC	160	VSS	226	DQ19_B
32	VSS	98	VSS	162	CA1_B	228	VSS
34	DQ09_A	100	NC	164	CA0_B	230	DQS2_B_c
36	VSS	102	NC	166	VSS	232	DQS2_B_t
38	DQ11_A	104	VSS	168	NC	234	VSS
40	VSS	106	CS0_A_n	170	VSS	236	DQ21_B
42	DM1_A_n	108	ALERT_n	172	NC	238	VSS
44	VSS	110	NC	174	VSS	240	DQ23_B
46	DQ13_A	112	VSS	176	NC	242	VSS
48	VSS	114	CA3_A	178	VSS	244	DQ25_B
50	DQ15_A	116	CA5_A	180	DQ1_B	246	VSS
52	VSS	118	VSS	182	VSS	248	DQ27_B
54	DQ17_A	120	CA7_A	184	DQ3_B	250	VSS
56	VSS	122	CA9_A	186	VSS	252	DM3_B_n
58	DQ19_A	124	VSS	188	DQS0_B_c	254	VSS
60	VSS	126	CA11_A	190	DQS0_B_t	256	DQ29_B
62	DQS2_A_c	**Key**		192	VSS	258	VSS
64	DQS2_A_t	128	RFU	194	DQ5_B	260	DQ31_B
66	VSS	130	VSS	196	VSS	262	VSS

Block Diagram





Note 1. ZQ Resistors are 240Ω ±1%.

Operating Conditions

Symbol	Parameter	MIN	Nom	MAX	Units	Note
VIN_BULK	Host Bulk input supply voltage	4.25	5.0	5.5	V	1
VIN_BULK Ramp_Up	Bulk input supply voltage ramp up rate	0.1	-	3.0	V/ms	2
VIN_BULK Ramp_Down	Bulk input supply voltage ramp down rate	0.5	-	1.0	V/ms	3

Notes:
1. During first power-on, the input voltage supply must reach a minimum of 4.25V for the PMIC to detect a valid input supply.
2. The ramp up rate is between 300mV and 4.0V.
3. The ramp down rate is between 4.0V and 300mV.

Recommended Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Note
TOPER	Normal Temperature Range	0 to 85	℃	1,2,3
	Extended Temperature Range (optional)	85 to 95	℃	1,3,4

Notes:
1. All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. All DDR5 SDRDAMs are required to operate in the temperature ranges.
4. When operating above 85℃, the host shall provide appropriate Refresh mode controls associated with the increased temperature range.

Absolute Maximum DC Ratings

Symbol	Parameter	MIN	MAX	Units	Note
VIN_BULK	Host Bulk input supply voltage (5V power input supply to the PMIC)	-0.3	6.0	V	1
HSCL & HSDA	Host SidebandBus clock & data (I2C Mode Only)	-0.5	3.6	V	1
	Host SidebandBus clock & data (I3C Mode Only)	-0.5	2.1	V	1
HSA	Host SidebandBus address	-0.5	2.1	V	1
TSTG	Storage Temperature	-55	100	℃	2

Notes:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Serial Presence Detect

Byte	Byte Description	Notes	Value(Hex)
0	Number of Bytes in SPD Device and Beta Level	1024Bytes	30
1	SPD Revision for Base Configuration Parameters	Rev. 1.0	10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	12
3	Key Byte / Module Type	Not hybrid, SO-DIMM	03
4	First SDRAM Density and Package	Monolithic SDRAM, 16Gb	04
5	First SDRAM Addressing	16 rows, 10 columns	00
6	First SDRAM I/O Width	x16	40
7	First SDRAM Bank Groups and Banks Per Bank Group	4 bank groups, 4 banks per bank group	42
8	Second SDRAM Density and Package	Symmetrical system	00
9	Second SDRAM Addressing	Symmetrical system	00
10	Second SDRAM I/O Width	Symmetrical system	00
11	Second SDRAM Bank Groups and Banks Per Bank Group	Symmetrical system	00
12	SDRAM BL32 and Post Package Repair	BL32 supported, One repair element per bank group	10
13	SDRAM Duty Cycle Adjuster and Partial Array Self Refresh	Device supports DCA for 4-phase internal clocks	02
14	SDRAM Fault Handling and Temperature Sense	Bounded Fault supported, Writeback suppression supported	05
15	Reserved	-	00
16	SDRAM Nominal Voltage, VDD	1.1V	00
17	SDRAM Nominal Voltage, VDDQ	1.1V	00
18	SDRAM Nominal Voltage, VPP	1.8V	00
19	SDRAM Timing	-	00
20	SDRAM Minimum Cycle Time (tCKAVGmin), LSB	tCKAVGmin=416ps	A0
21	SDRAM Minimum Cycle Time (tCKAVGmin), MSB	tCKAVGmin=416ps	01
22	SDRAM Maximum Cycle Time (tCKAVGmax), LSB	tCKAVGmax=1010ps	F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), MSB	tCKAVGmax=1010ps	03
24	CAS Latencies Supported, First Byte	CL=22,26,28,30,32,36,40,42	7A
25	CAS Latencies Supported, Second Byte	CL=22,26,28,30,32,36,40,42	0D
26	CAS Latencies Supported, Third Byte	CL=22,26,28,30,32,36,40,42	00
27	CAS Latencies Supported, Fourth Byte	CL=22,26,28,30,32,36,40,42	00
28	CAS Latencies Supported, Fifth Byte	CL=22,26,28,30,32,36,40,42	00
29	Reserved	-	00
30	SDRAM Read Command to First Data (tAA), LSB	tAAmin=16000ps	80
31	SDRAM Read Command to First Data (tAA), MSB	tAAmin=16000ps	3E
32	SDRAM Activate to Read or Write Command Delay (tRCD), LSB	tRCDmin=16000ps	80
33	SDRAM Activate to Read or Write Command Delay (tRCD), MSB	tRCDmin=16000ps	3E
34	SDRAM Row Precharge Time (tRP), LSB	tRPmin=16000ps	80
35	SDRAM Row Precharge Time (tRP), MSB	tRPmin=16000ps	3E
36	SDRAM Activate to Precharge Command Period (tRAS), LSB	tRASmin=32000ps	00
37	SDRAM Activate to Precharge Command Period (tRAS), MSB	tRASmin=32000ps	7D
38	SDRAM Activate to Activate or Refresh Command Period (tRC), LSB	tRCmin=48000ps	80
39	SDRAM Activate to Activate or Refresh Command Period (tRC), MSB	tRCmin=48000ps	BB
40	SDRAM Write Recovery Time (tWR), LSB	tWRmin=30000ps	30
41	SDRAM Write Recovery Time (tWR), MSB	tWRmin=30000ps	75
42	SDRAM Normal Refresh Recovery Time (tRFC1, tRFC1_slr), LSB	tRFC1min=295ns	27
43	SDRAM Normal Refresh Recovery Time (tRFC1, tRFC1_slr), MSB	tRFC1min=295ns	01
44	SDRAM Fine Granularity Refresh Recovery Time (tRFC2, tRFC2_slr), LSB	tRFC2min=160ns	A0
45	SDRAM Fine Granularity Refresh Recovery Time (tRFC2, tRFC2_slr), MSB	tRFC2min=160ns	00
46	SDRAM Same Bank Refresh Recovery Time (tRFCsb, tRFCsb_slr), LSB	tRFCsbmin=130ns	82
47	SDRAM Same Bank Refresh Recovery Time (tRFCsb, tRFCsb_slr), MSB	tRFCsbmin=130ns	00
48	SDRAM Normal Refresh Recovery Time, 3DS Different Logical Rank (tRFC1_dlr), LSB	-	00
49	SDRAM Normal Refresh Recovery Time, 3DS Different Logical Rank (tRFC1_dlr), MSB	-	00
50	SDRAM Fine Granularity Refresh Recovery Time, 3DS Different Logical Rank (tRFC2_dlr), LSB	-	00
51	SDRAM Fine Granularity Refresh Recovery Time, 3DS Different Logical Rank (tRFC2_dlr), MSB	-	00
52	SDRAM Same Bank Refresh Recovery Time, 3DS Different Logical Rank (tRFCsb_dlr), LSB	-	00
53	SDRAM Same Bank Refresh Recovery Time, 3DS Different Logical Rank (tRFCsb_dlr), MSB	-	00

Serial Presence Detect

Byte	Byte Description	Notes	Value(Hex)
54	SDRAM Refresh Management, First Byte, First SDRAM	-	00
55	SDRAM Refresh Management, Second Byte, First SDRAM	-	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	-	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	-	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	-	00
59	SDRAM Adaptive Refresh Management, Level A, Second Byte, First SDRAM	-	00
60	SDRAM Adaptive Refresh Management, Level A, First Byte, Second SDRAM	-	00
61	SDRAM Adaptive Refresh Management, Level A, Second Byte, Second SDRAM	-	00
62	SDRAM Adaptive Refresh Management, Level B, First Byte, First SDRAM	-	00
63	SDRAM Adaptive Refresh Management, Level B, Second Byte, First SDRAM	-	00
64	SDRAM Adaptive Refresh Management, Level B, First Byte, Second SDRAM	-	00
65	SDRAM Adaptive Refresh Management, Level B, Second Byte, Second SDRAM	-	00
66	SDRAM Adaptive Refresh Management, Level C, First Byte, First SDRAM	-	00
67	SDRAM Adaptive Refresh Management, Level C, Second Byte, First SDRAM	-	00
68	SDRAM Adaptive Refresh Management, Level C, First Byte, Second SDRAM	-	00
69	SDRAM Adaptive Refresh Management, Level C, Second Byte, Second SDRAM	-	00
70	SDRAM Activate to Activate Command Delay for Same Bank Group (tRRD_L), LSB	tRRD_Lmin=5000ps	88
71	SDRAM Activate to Activate Command Delay for Same Bank Group (tRRD_L), MSB	tRRD_Lmin=5000ps	13
72	SDRAM Activate to Activate Command Delay for Same Bank Group (tRRD_L), Lower Clock Limit	8CK	08
73	SDRAM Read to Read Command Delay for Same Bank Group (tCCD_L), LSB	tCCD_Lmin=5000ps	88
74	SDRAM Read to Read Command Delay for Same Bank Group (tCCD_L), MSB	tCCD_Lmin=5000ps	13
75	SDRAM Read to Read Command Delay for Same Bank Group (tCCD_L), Lower Clock Limit	8CK	08
76	SDRAM Write to Write Command Delay for Same Bank Group (tCCD_L_WR), LSB	tCCD_L_WRmin=20000ps	20
77	SDRAM Write to Write Command Delay for Same Bank Group (tCCD_L_WR), MSB	tCCD_L_WRmin=20000ps	4E
78	SDRAM Write to Write Command Delay for Same Bank Group (tCCD_L_WR), Lower Clock Limit	32CK	20
79	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW (tCCD_L_WR2), LSB	tCCD_L_WR2min=10000ps	10
80	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW (tCCD_L_WR2), MSB	tCCD_L_WR2min=10000ps	27
81	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW (tCCD_L_WR2), Lower Clock Limit	16CK	10
82	SDRAM Four Activate Window (tFAW), LSB	tFAWmin=16666ps	1A
83	SDRAM Four Activate Window (tFAW), MSB	tFAWmin=16666ps	41
84	SDRAM Four Activate Window (tFAW), Lower Clock Limit	40K	28
85	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), LSB	tCCD_L_WTRmin=10000ps	10
86	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), MSB	tCCD_L_WTRmin=10000ps	27
87	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), Lower Clock Limit	16CK	10
88	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), LSB	tCCD_S_WTRmin=2500ps	C4
89	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), MSB	tCCD_S_WTRmin=2500ps	09
90	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), Lower Clock Limit	4CK	04

Serial Presence Detect

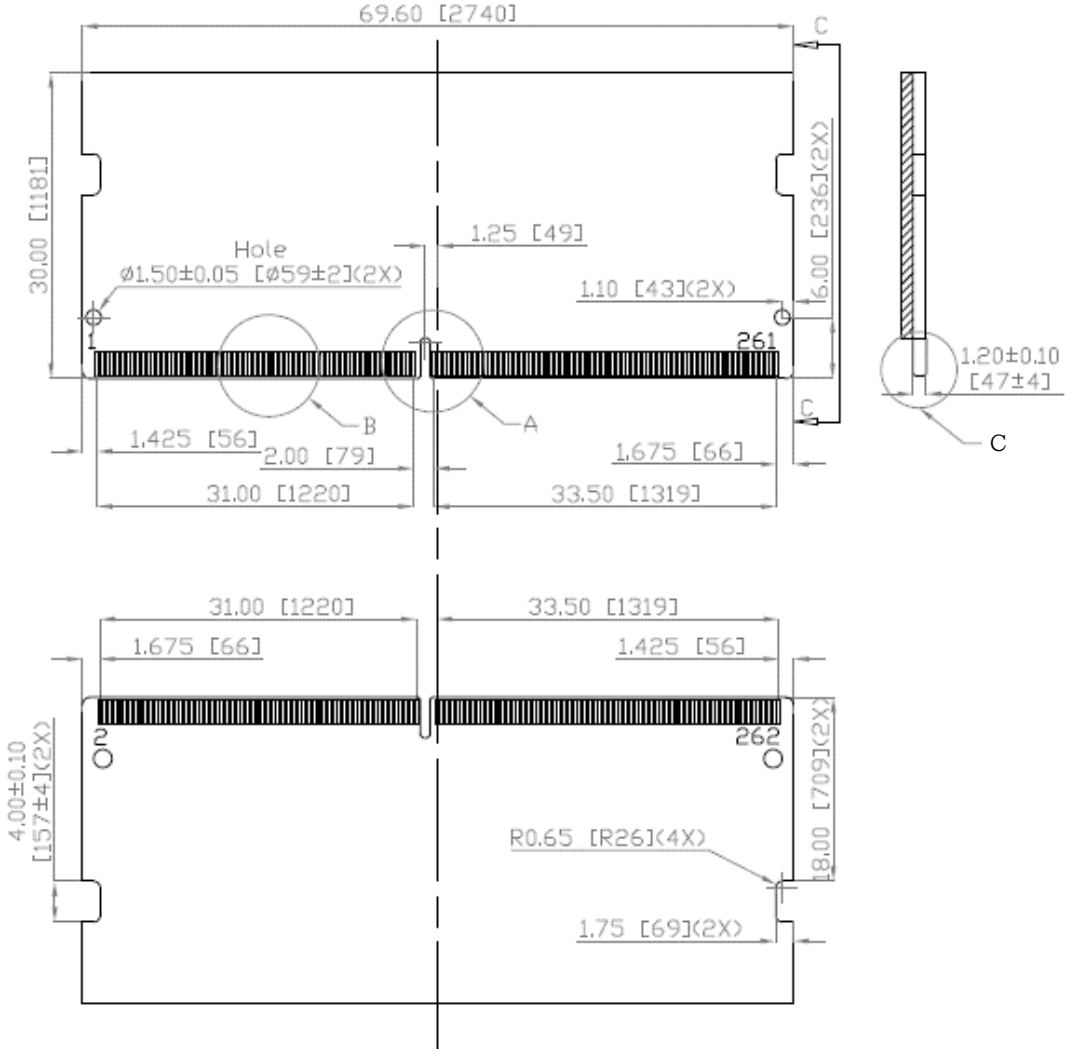
Byte	Byte Description	Notes	Value(Hex)
91	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), LSB	tRTPmin=7500ps	4C
92	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), MSB	tRTPmin=7500ps	1D
93	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Lower Clock Limit	12CK	0C
94~127	Reserved, Base Configuration Section	-	00
128~191	Reserved for future use	-	00
192	SPD Revision for Module Information byte 192~447	Rev. 1.0	10
193	Hashing Sequence	-	00
194	SPD Manufacturer ID Code, First Byte	Renesas(IDT)	80
195	SPD Manufacturer ID Code, Second Byte	Renesas(IDT)	B3
196	SPD Device Type	SPD5118	80
197	SPD Device Revision Number	B1	21
198	PMIC 0 Manufacturer ID Code, First Byte	Richtek	8A
199	PMIC 0 Manufacturer ID Code, Second Byte	Richtek	8C
200	PMIC 0 Device Type	PMIC5100	82
201	PMIC 0 Revision Number	51	51
202	PMIC 1 Manufacturer ID Code, First Byte	-	00
203	PMIC 1 Manufacturer ID Code, Second Byte	-	00
204	PMIC 1 Device Type	-	00
205	PMIC 1 Revision Number	-	00
206	PMIC 2 Manufacturer ID Code, First Byte	-	00
207	PMIC 2 Manufacturer ID Code, Second Byte	-	00
208	PMIC 2 Device Type	-	00
209	PMIC 2 Revision Number	-	00
210	Thermal Sensor Manufacturer ID Code, First Byte	-	00
211	Thermal Sensor Manufacturer ID Code, Second Byte	-	00
212	Thermal Sensor Device Type	-	00
213	Thermal Sensor Revision Number	-	00
214~229	Reserved	-	00
230	Module Nominal Height	SODIMM	0F
231	Module Maximum Thickness	SODIMM	01
232	Reference Raw Card Used	Raw Card C0	02
233	DIMM Attributes	XT, Extended Grade (1Row)	81
234	Module Organization	Symmetrical, 1 PKG Rank	00
235	Memory Channel Bus Width	SODIMM	22
236~239	Reserved	-	00
240~447	Module Type Specific Information	-	00
448~509	Reserved for future use	-	00
510-511	Cyclical Redundancy Code (CRC) for SPD Bytes 0~509	-	C6 58
512	Module Manufacturer's ID Code, First Byte	ADTEC Corporation	02
513	Module Manufacturer's ID Code, Second Byte		29
514	Module Manufacturing Location	Japan	01
515	Year of Manufacture (BCD)	(e.g.) Year 2024	24
516	Week of Manufacture (BCD)	(e.g.) Week 01	01
517	Module Serial Number	(e.g.) S/N: 00000000	00
518			00
519			00
520			00

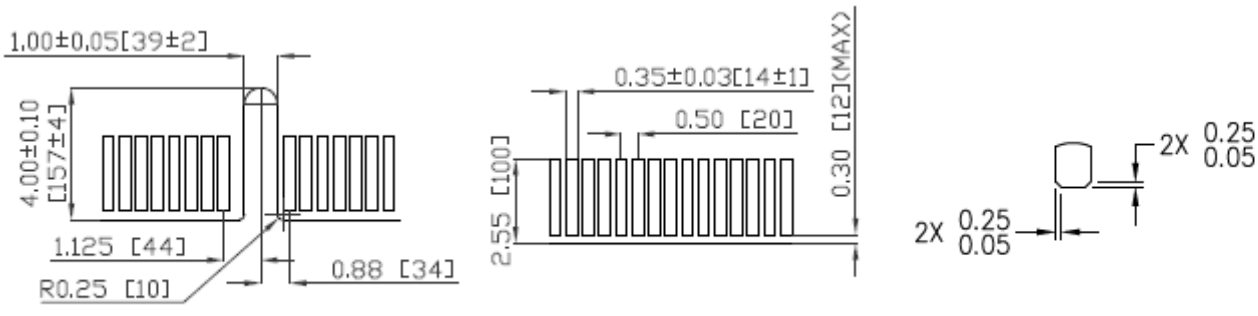
Serial Presence Detect

Byte	Byte Description	Notes	Value(Hex)
521	Module Part Number in ASCII Code	(e.g.) 4	34
522		(e.g.) 8	38
523		(e.g.) 0	30
524		(e.g.) 0	30
525		(e.g.) S	53
526		(e.g.) 0	30
527		(e.g.) 8	38
528		(e.g.) G	47
529		(e.g.) 1	31
530		(e.g.) 6	36
531		(e.g.) 5	35
532		(e.g.) H	48
533		(e.g.) A	41
534			20
535			20
536			20
537			20
538			20
539			20
540			20
541			20
542			20
543			20
544			20
545			20
546			20
547			20
548			20
549			20
550			20
551	Module Revision Code		00
552	DRAM Manufacturer's ID Code, First Byte	(e.g.) SK Hynix	80
553	DRAM Manufacturer's ID Code, Second Byte		AD
554	DRAM Stepping	(e.g.) A	41
555	Manufacturer's Specific Data		00
556-637			00
638-1023	Reserved		00

Outline Dimensions

Unit : mm
Tolerance : ±0.15





Detail A　　Detail B　　Detail C